A EuroHPC project

Network Solution

for Exascale Architectures

ENABLE

Enable the design of a new generation of high-performance network interconnect

EXPLORE

Explore new innovative solutions

DEVELOP

Develop the ecosystem and create a broader community of users and developers

WHO WE ARE

The RED-SEA project prepares a new-generation of European Network Interconnect, capable of powering the EU Exascale systems to come, leveraging efficient European interconnect technology (BXI) associated with a standard and mature technology (Ethernet), in full coordination with other EU-funded initiatives. RED-SEA brings together the top European academic centres and the key European industrial forces in the domain of interconnect networks, with a consortium gathering 12 partners from 6 countries.

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CONTEXT

Network interconnects play an enabling role in HPC systems – and this will be even truer for the coming Exascale systems that will rely on higher node counts and increased use of parallelism and communication. Moreover, next-generation HPC and data-driven systems will be powered by heterogeneous computing devices, including low-power Arm and RISC-V processors, high-end CPUs, vector acceleration units and GPUs suitable for massive single-instruction multiple-data (SIMD) workloads, as well as FPGA and ASIC designs tailored for extremely power-efficient custom codes.

These compute units will be surrounded by distributed, heterogeneous (often deep) memory hierarchies, including high-bandwidth memories and fast devices offering microsecond-level access time. At the same time, modern data-parallel processing units such as GPUs and vector accelerators can crunch data at amazing rates (tens of TFLOPS). In this landscape, the network may well become the next big bottleneck, similar to memory in single node systems.

THE RED-SEA CONTRIBUTION

RED-SEA will build upon the European interconnect BXI (BullSequana eXascale Interconnect), together with standard and mature technology (Ethernet) and previous EU-funded initiatives to provide a competitive and efficient network solution for the exascale era and beyond. This involves developing the key IPs and the software environment that will deliver:

- scalability, while maintaining an acceptable total cost of ownership and power efficiency;
- virtualization and security, to allow various applications to efficiently and safely share an HPC system;
- Quality-of-service and congestion management to make it possible to share the platform among users and applications with different demands;
- reliability at scale, because fault tolerance is a key concern in a system with a very large number of components;
- support of high-bandwidth low-latency HPC Ethernet, as HPC systems increasingly need to interact securely with the outside world, including public clouds, edge servers or third party HPC systems;
- support of heterogeneous programming model and runtimes to facilitate the convergence of HPC and HPDA;
- support for low-power processors and accelerators.

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